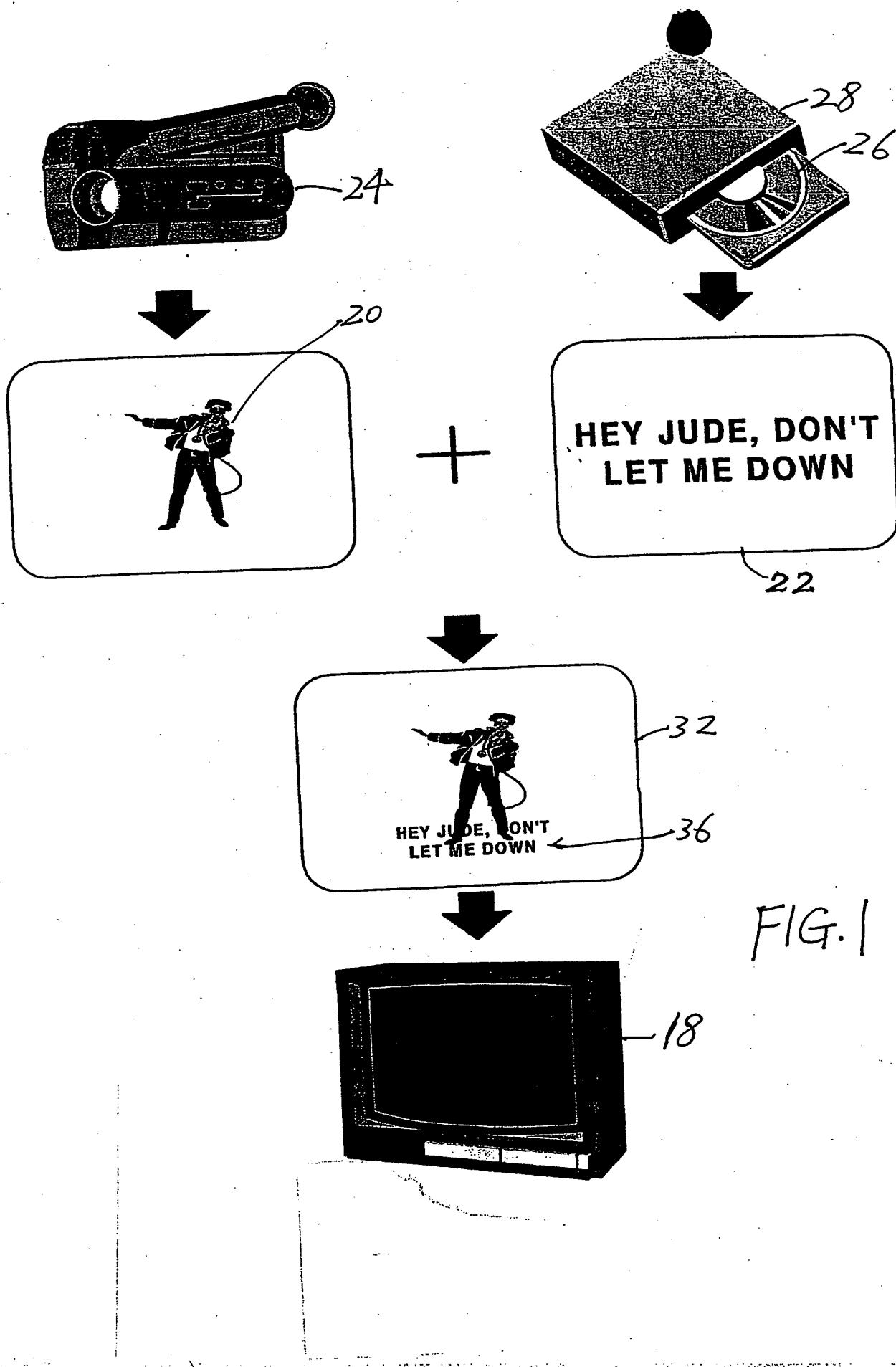


001ET2AT 9005932650



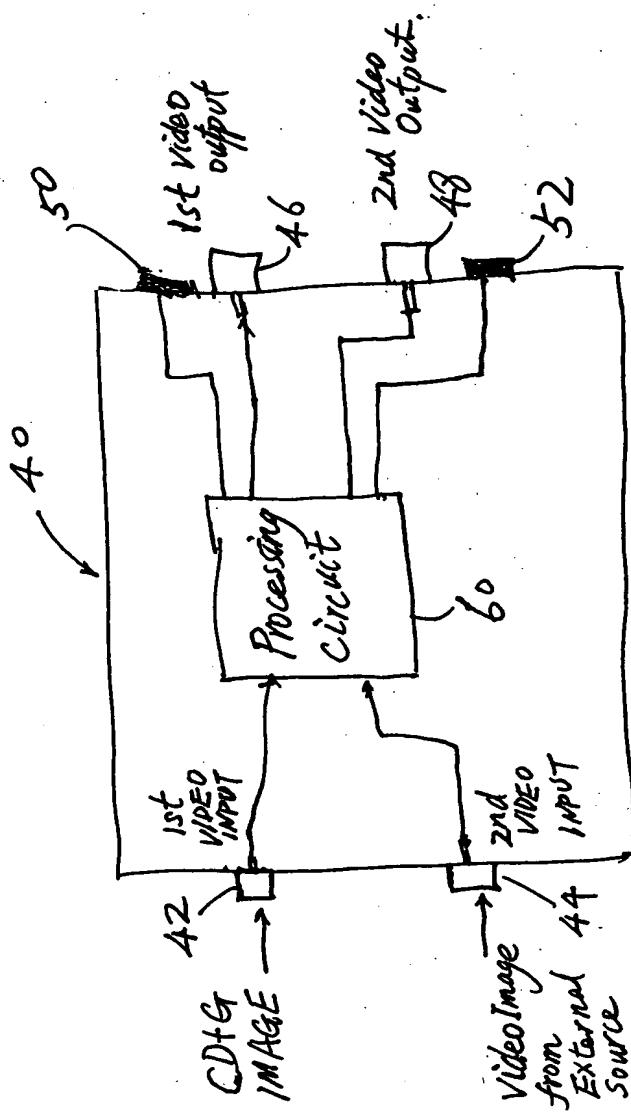


FIG. 2

000000000000000000000000

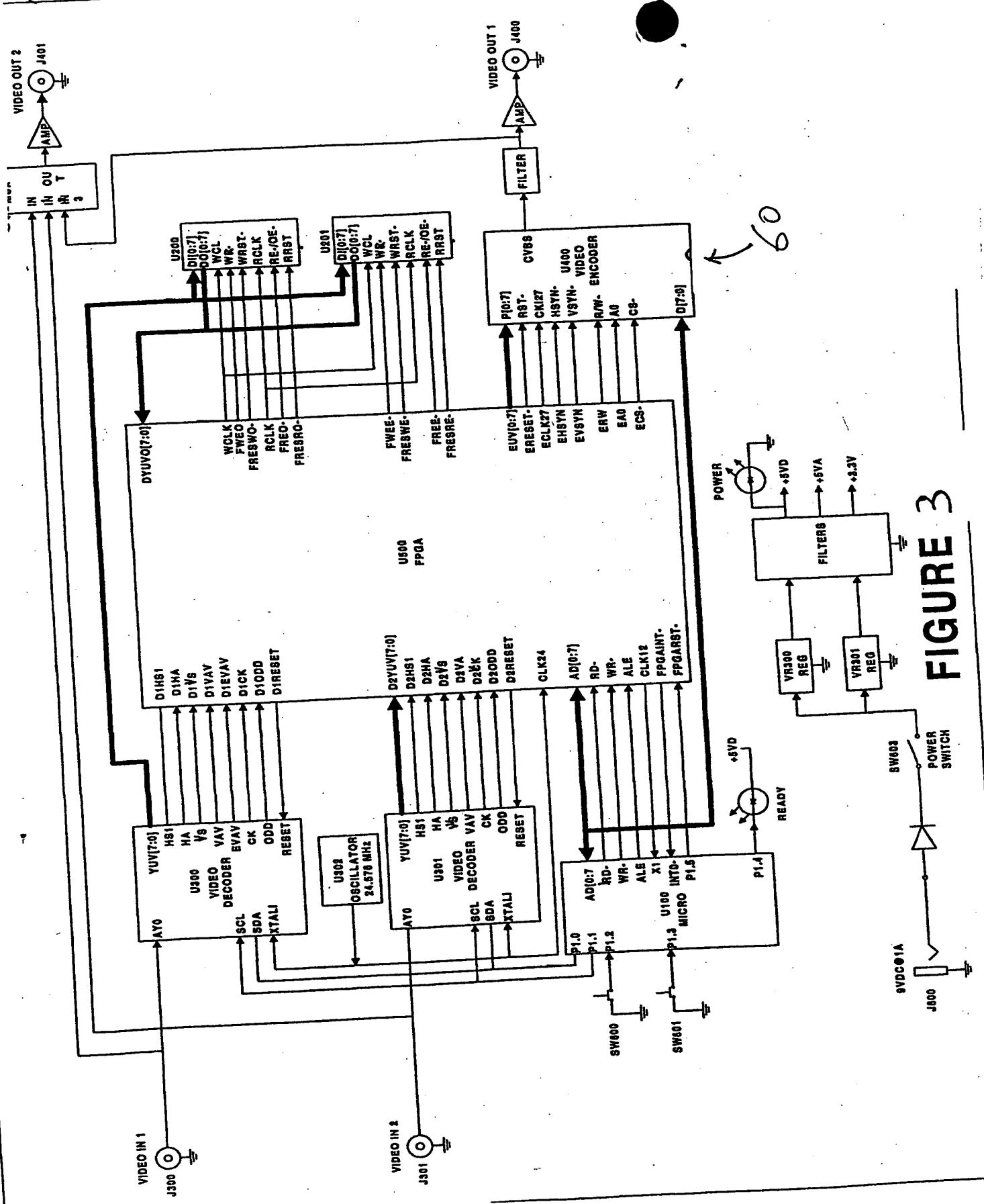
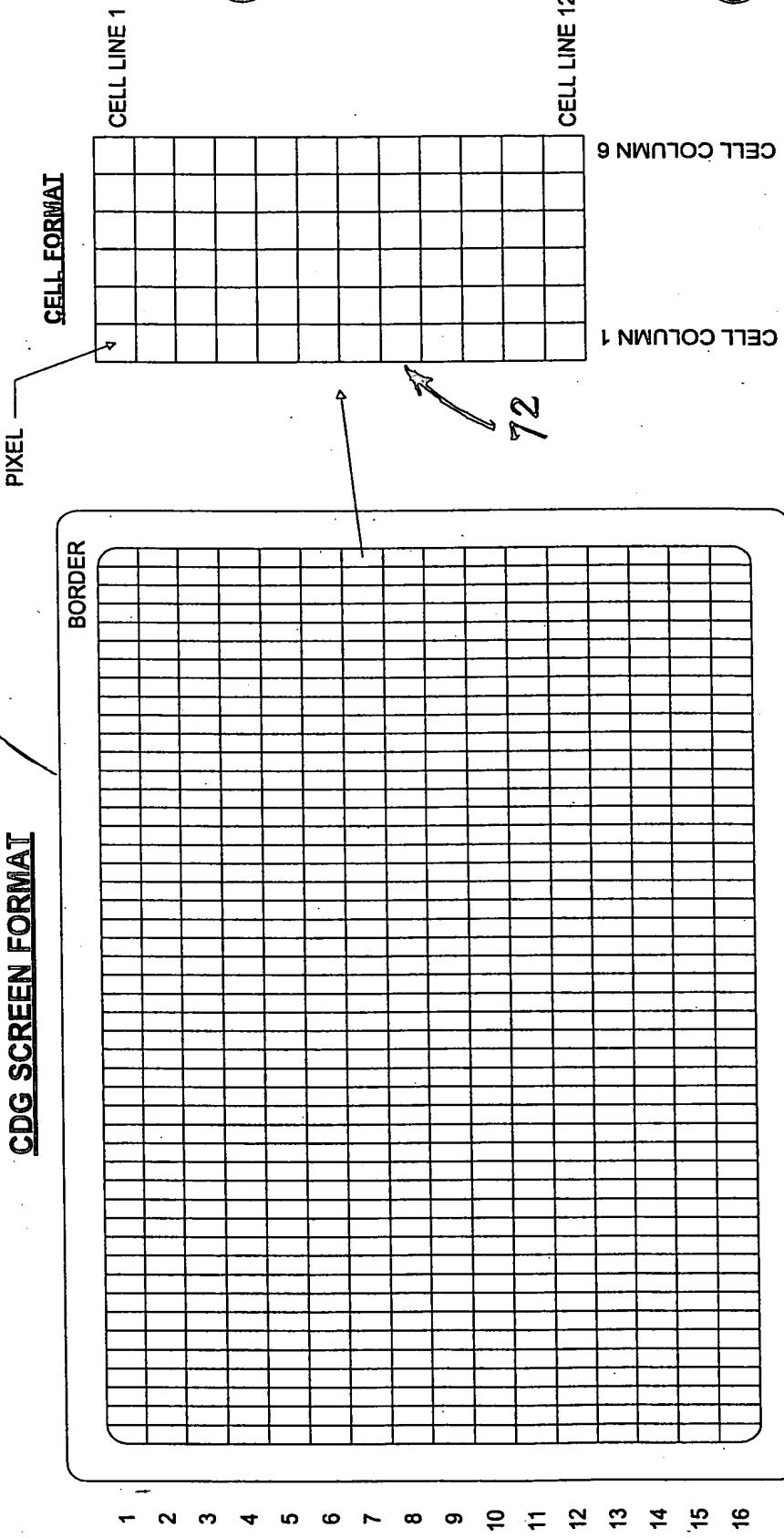


FIGURE 3

70



1

48

FIG. 4

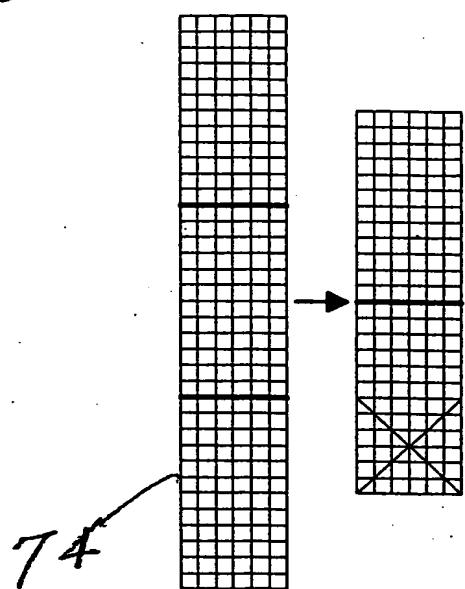


FIG.5

09246906 1121200

CELL START POSITION TRANSLATION	
INPUT CELL LINE	OUTPUT CELL LINE START
1	9
2	9.5
3	10
4	10.5
5	11
6	11.5
7	12
8	12.5
9	13
10	13.5
11	14
12	14.5
13	15
14	15.5
15	16
16	16.5

76

FIG.6

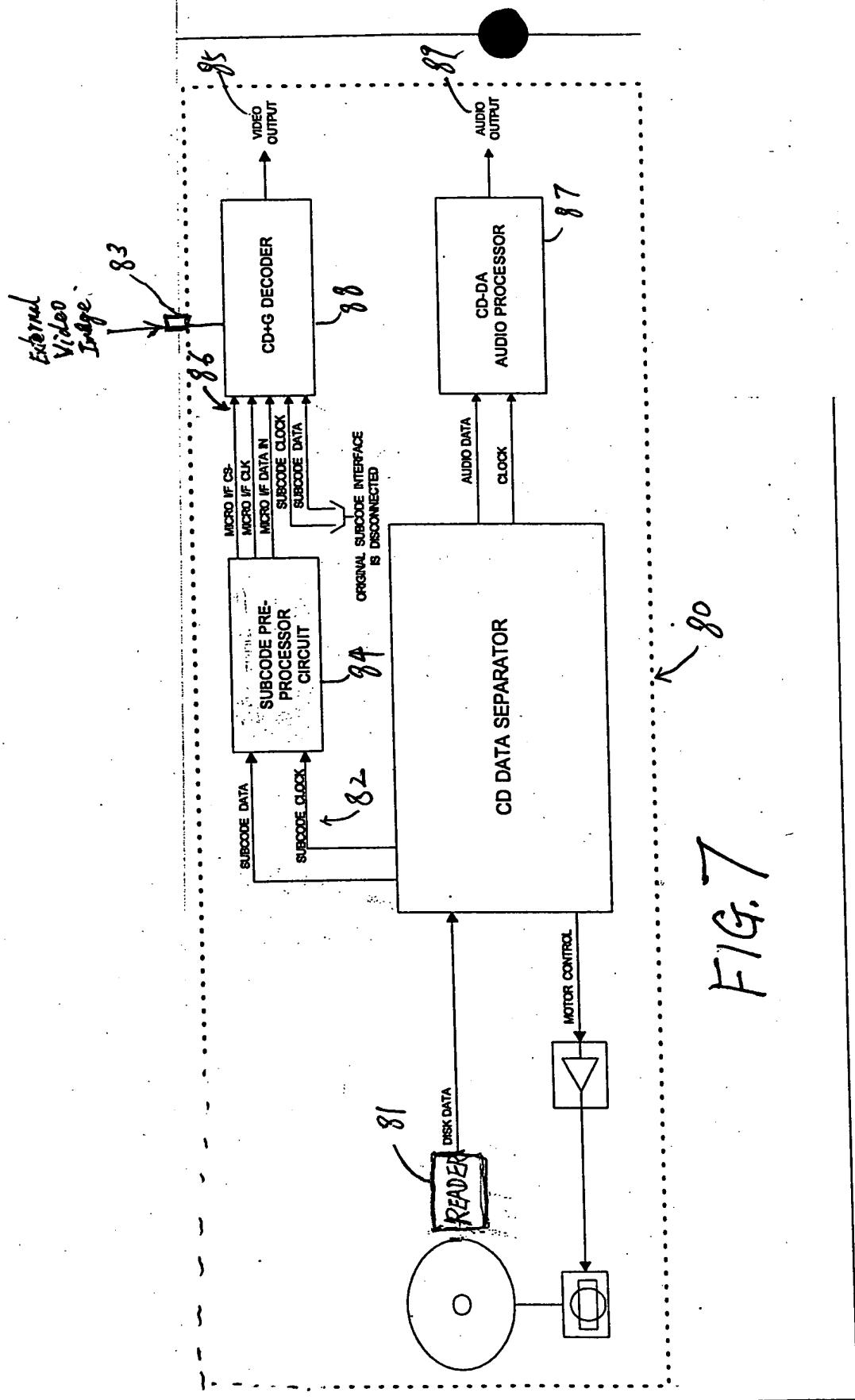
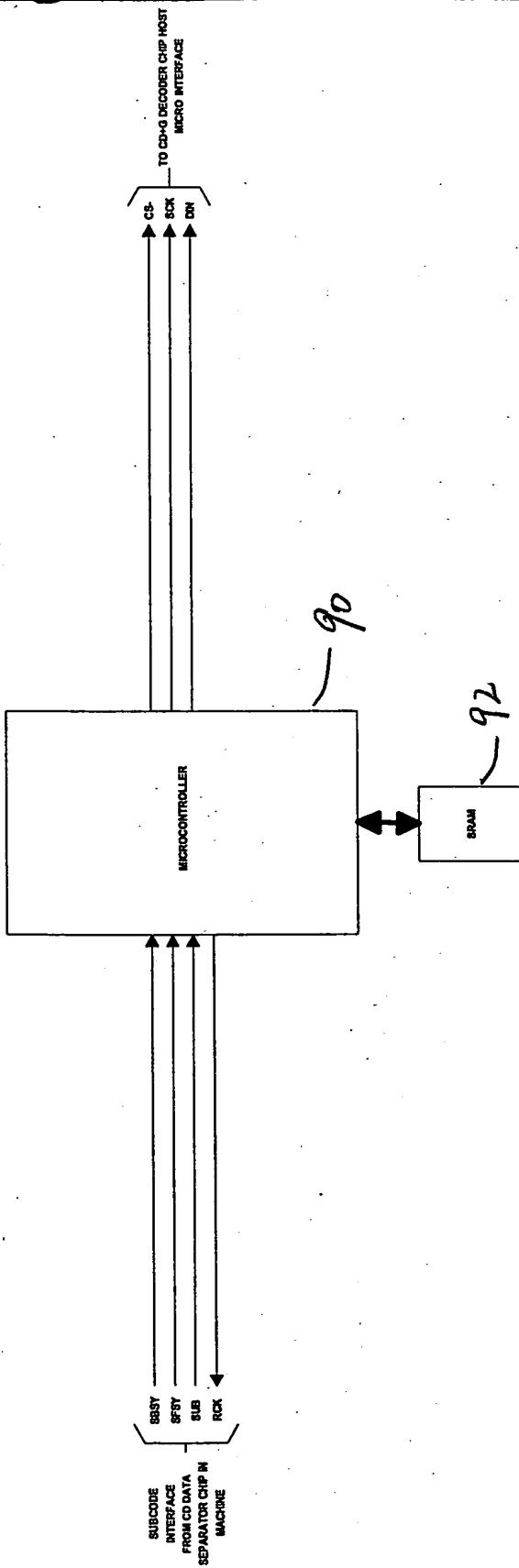


FIG. 7

SUBCODE PRE-PROCESSOR CIRCUIT

✓ 84



F16.8

0926906 121200

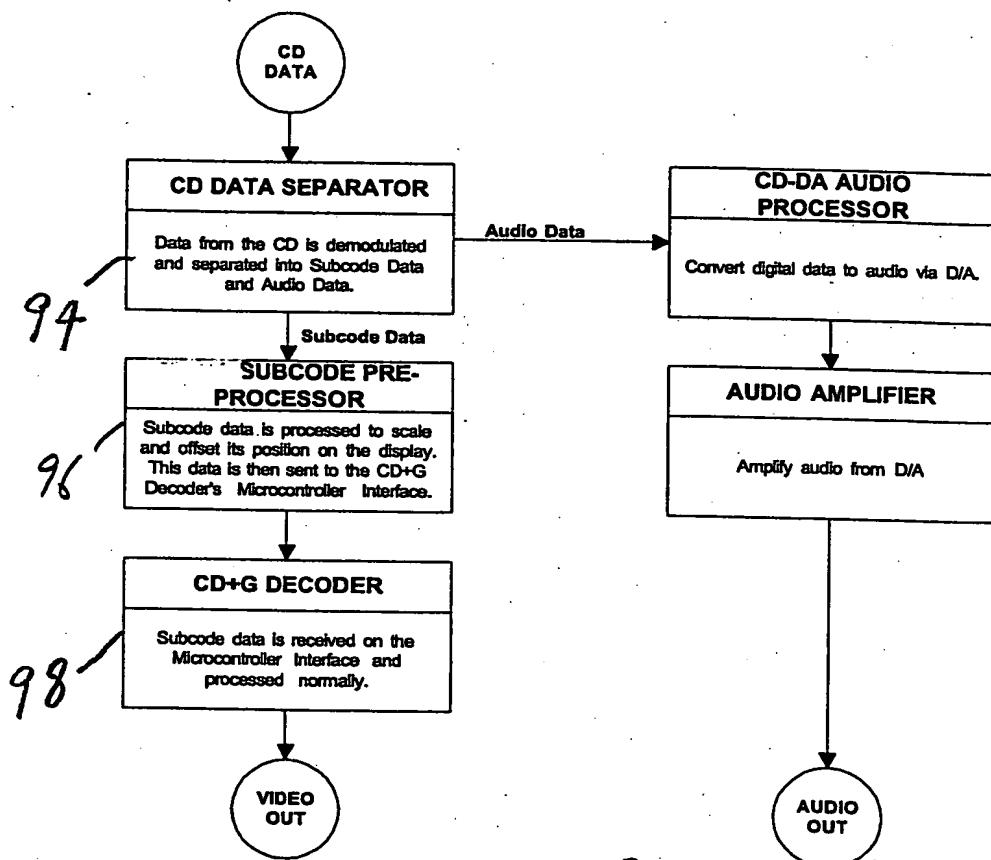


FIG. 9

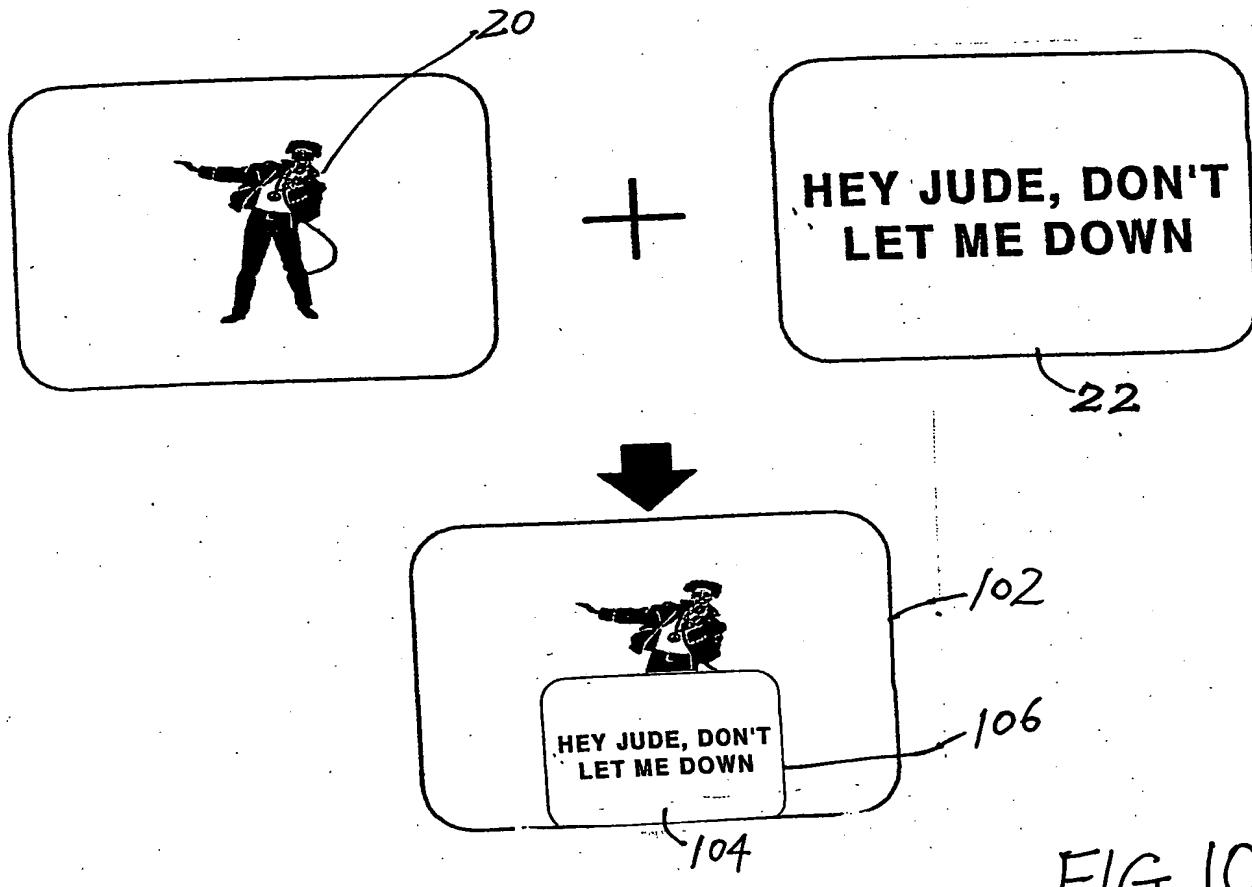


FIG. 10